WHAT IS CLAIMED IS:

1. A semiconductor component comprising:

a semiconductor die comprising an electrically insulating layer and a plurality of die contacts;

a capacitor on die comprising a first electrode on the electrically insulating layer in electrical communication with a first die contact, a dielectric layer on the first electrode, and a second electrode on the dielectric layer in electrical communication with a second die contact;

a first terminal contact on the die in electrical communication with the first electrode, and a second terminal contact on the die in electrical communication with the second electrode; and

a protective layer on the die encapsulating the capacitor.

2. The component of claim 1 wherein the first electrode comprises a first redistribution layer on the die.

3. The component of claim 1 wherein the second electrode comprises a second redistribution layer on the die.

4. The component of claim 1 wherein the first die contact comprises a ground contact for the die.

5. The component of claim 1 wherein the second die contact comprises a power contact for the die.

6. The component of claim 1 wherein the die contacts comprise bond pads.

7. The component of claim 1 wherein the electrically insulating layer comprises a passivation layer.

8. The component of claim 1 wherein the component further comprises a plurality of terminal contacts on the die comprising balls or bumps in a grid array.

9. A semiconductor component comprising:

a semiconductor die;

a capacitor comprising a first electrode comprising a portion of a first redistribution layer on the die, a dielectric layer on the first electrode, and a second electrode on the dielectric layer comprising a portion of a second redistribution layer on the die; and

a first terminal contact on the die in electrical communication with the first electrode, and a second terminal contact on the die in electrical communication with the second electrode.

10. The component of claim 9 further comprising a protective layer on the die encapsulating the capacitor.

11. The component of claim 9 wherein the first die contact comprises a ground contact for the die.

12. The component of claim 9 wherein the second die contact comprises a power contact for the die.

13. The component of claim 9 wherein the first terminal contact and the second terminal contact comprise elements of a ball grid array.

14. A semiconductor component comprising:

a semiconductor die comprising a plurality of integrated circuits and a plurality of die contacts in electrical communication with the integrated circuits;

an on board capacitor on die configured to filter transient voltages, spurious signals, and power supply noise in signals transmitted to the integrated circuits, the capacitor comprising a first electrode on the die in electrical communication with a ground die contact, a dielectric layer on the first electrode, and a second electrode on the dielectric layer in electrical communication with a power die contact; and

a plurality of terminal contacts on the die in electrical communication with the die contacts, including a ground terminal contact in electrical communication with the first electrode, and a power terminal contact in electrical communication with the second electrode.

15. The component of claim 14 further comprising a protective layer on the die encapsulating the capacitor.

16. The component of claim 14 wherein the terminal contacts comprise bumps or balls in a grid array.

17. The component of claim 14 wherein the first electrode comprises a first redistribution layer on the die.

18. The component of claim 14 wherein the second electrode comprises a second redistribution layer on the die.

19. The component of claim 14 further comprising a ground conductor on the die in electrical communication with the ground die contact and the first electrode.

20. The component of claim 14 further comprising a plurality of conductors on the die in electrical communication with the die contacts and the terminal contacts comprising portions of a redistribution layer.

21. The component of claim 14 wherein the component comprises a package.

22. The component of claim 14 wherein the die is contained on a semiconductor wafer comprising a plurality of dice identical to the die.

23. A semiconductor component comprising:

a semiconductor wafer comprising a plurality of semiconductor dice;

a first redistribution layer on the wafer and a second redistribution layer on the wafer;

an on board capacitor on each die, each capacitor comprising a first electrode comprising a portion of the first redistribution layer on the die, a dielectric layer on the first electrode, and a second electrode on the dielectric layer comprising a portion of the second redistribution layer on the die.

24. The component of claim 23 further comprising a plurality of terminal contacts on the dice comprising bumps or balls in a grid array.

25. The component of claim 23 further comprising a ground terminal contact on each die in electrical communication with the first electrode, and a power terminal contact on each die in electrical communication with the second electrode.

26. A method for fabricating a semiconductor component comprising:

providing a semiconductor die comprising an electrically insulating layer and a plurality of die contacts;

forming a first electrode on the electrically insulating layer in electrical communication with a first die contact;

forming a dielectric layer on the first electrode;

forming a second electrode on the dielectric layer in electrical communication with a second die contact;

forming a first terminal contact on the die in electrical communication with the first electrode;

forming a second terminal contact on the die in electrical communication with the second electrode; and

forming a protective layer on the die encapsulating the first electrode, the dielectric layer and the second electrode.

27. The method of claim 26 wherein the forming the first electrode step comprises patterning a first redistribution layer on the die.

28. The method of claim 26 wherein the forming the second electrode step comprises patterning a second redistribution layer on the die.

29. The method of claim 26 wherein the first die contact comprises a ground contact for the die.

30. The method of claim 26 wherein the second die contact comprises a power contact for the die.

31. The method of claim 26 wherein the die contacts comprise bond pads.

32. The method of claim 26 wherein the electrically insulating layer comprises a passivation layer.

33. The method of claim 26 wherein the terminal contacts comprise bumps or balls in a grid array.

34. A method for fabricating a semiconductor component with an on board capacitor comprising:

providing a semiconductor die comprising a plurality of die contacts;

forming a first redistribution layer on the die;

patterning the first redistribution layer to form a first electrode of the capacitor in electrical communication with a first die contact;

forming a dielectric layer of the capacitor on the first electrode;

forming a second redistribution layer on the die and on the dielectric layer; and

patterning the second redistribution layer to form a second electrode of the capacitor in electrical communication with a second die contact.

35. The method of claim 34 further comprising forming a first terminal contact on the die in electrical communication with the first electrode.

36. The method of claim 34 further comprising forming a second terminal contact on the die in electrical communication with the second electrode.

37. The method of claim 34 further comprising forming a protective layer on the die encapsulating the first electrode, the dielectric layer and the second electrode.

38. The method of claim 34 wherein the first die contact comprises a ground contact and the second die contact comprises a power contact.

39. A method for fabricating a semiconductor component with an on board capacitor comprising:

providing a semiconductor die comprising a plurality of integrated circuits and a plurality of die contacts in electrical communication with the integrated circuits;

forming an on board capacitor on die by forming a first electrode on the die in electrical communication with a ground die contact, a dielectric layer on the first electrode, and a second electrode on the dielectric layer in electrical communication with a power die contact; and

forming a plurality of terminal contacts on the die in electrical communication with the die contacts, including a ground terminal contact in electrical communication with the first electrode, and a power terminal contact in electrical communication with the second electrode.

40. The method of claim 39 further comprising forming a protective layer on the die encapsulating the capacitor.

41. The method of claim 39 wherein the terminal contacts comprise bumps or balls in a grid array.

42. The method of claim 39 wherein forming the first electrode comprises patterning a first redistribution layer for the die.

43. The method of claim 39 wherein forming the second electrode comprises patterning a second redistribution layer for the die.

44. The method of claim 39 further comprising forming a ground conductor on the die in electrical communication with the ground die contact and the first electrode.

45. The method of claim 39 further comprising forming a plurality of conductors on the die in electrical communication with the die contacts and the terminal contacts comprising portions of a redistribution layer.

46. The method of claim 39 wherein the component comprises a package.

47. The method of claim 39 wherein the die is contained on a semiconductor wafer comprising a plurality of dice identical to the die.

48. A method for fabricating a semiconductor component with an on board capacitor comprising:

providing a semiconductor wafer containing a semiconductor die;

forming a first redistribution layer on the wafer;

forming a first electrode of the capacitor by patterning the first redistribution layer;

forming a dielectric layer on the first electrode;

forming a second redistribution layer on the wafer;

forming a second electrode on the dielectric layer by patterning the second redistribution layer; and

forming a protective layer on the wafer encapsulating the first electrode, the dielectric layer and the second electrode.

49. The method of claim 48 further comprising singulating the die from the wafer.

50. The method of claim 48 further comprising forming a plurality of terminal contacts on the die including a ground terminal contact in electrical communication with the first

electrode and a power terminal contact in electrical communication with the second electrode.

51. A system in a package comprising:

a substrate comprising a plurality of terminal leads; and

at least one component on the substrate comprising a plurality of terminal contacts in electrical communication with the terminal leads;

the component comprising a semiconductor die having a plurality of die contacts and an on board capacitor in electrical communication with the die contacts;

the capacitor comprising a first electrode in electrical communication with a first die contact and a first terminal contact, a dielectric layer on the first electrode, and a second electrode on the dielectric layer in electrical communication with a second die contact and a second terminal contact.

52. The system of claim 51 wherein the terminal contacts comprise bumps or balls bonded to the substrate.

53. The system of claim 51 wherein the first die contact comprises a ground contact for the die.

54. The system of claim 51 wherein the second die contact comprises a power contact for the die.

55. The system of claim 51 wherein the die contacts comprise bond pads.

56. The system of claim 51 further comprising a plastic body encapsulating the die.

57. An electronic system comprising:

a board comprising a plurality of electrodes;

a semiconductor wafer comprising a plurality of semiconductor dice having a plurality of integrated circuits;

each die comprising a plurality of terminal contacts bonded to the electrodes, and an on board capacitor configured to filter transient voltages, spurious signals, and power supply noise in signals transmitted to the integrated circuits,

the capacitor comprising a first electrode on the die in electrical communication with a first die contact and a first terminal contact, a dielectric layer on the first electrode, and a second electrode on the dielectric layer in electrical communication with a second die contact and a second terminal contact.

58. The system of claim 57 wherein the first die contact and the first terminal contact comprise ground contacts.

59. The system of claim 57 wherein the second die contact and the second terminal contact comprise power contacts.